

Amendments to the Drawings:

The attached replacement sheets of drawings includes changes to Figs. 2-2, 3 and 5, and replace the original sheets including Figs 2-2, 3 and 5.

In Figure 2-1, applicant changed the reference numeral 14, pointing to the multithreaded processor shown in the figure, to reference numeral 12. Applicant further removed reference numeral 56 which was pointing to the element block identified as "PLL GRAMMAR."

In Figure 2-2, applicant changed the reference numeral 29, pointing to the element block identified as the Scratch Pad, to reference numeral 27. Further, applicant replaced "SDRAM" with "SRAM" in element block 16b.

In Figure 3, the applicant marked the element identified as uPC\_1 with reference numeral 72a (which previously pointed to uPC\_4), uPC\_2 with reference numeral 72b (which previously pointed to uPC-1), and uPC\_3 with reference numeral 72c (which previously pointed to the illustrated multiplexer). Additionally, applicant added new reference numeral 72d to mark uPC\_4.

In Figure 5, applicant changed the notation "Srl" to "Src" and changed the notations of "P" to "I".

Attachments following last page of this Amendment:

Annotated Sheet Showing Change(s) (4 pages)

Replacement Sheet (6 pages)

REMARKS

Applicant thanks the examiner for his help in resolving the outstanding issues in relation to the previously submitted Information Disclosure Statements.

In response to the Notice of Allowability, dated August 23, 2006, applicant submits herewith a complete set of formal drawings. Applicant has amended Figs. 2-1, 2-2, 3 and 5 to correct typographical errors, to promote clarity, and to make the drawings consistent with the written description.

Please apply any required fees to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date:

November 17, 2006



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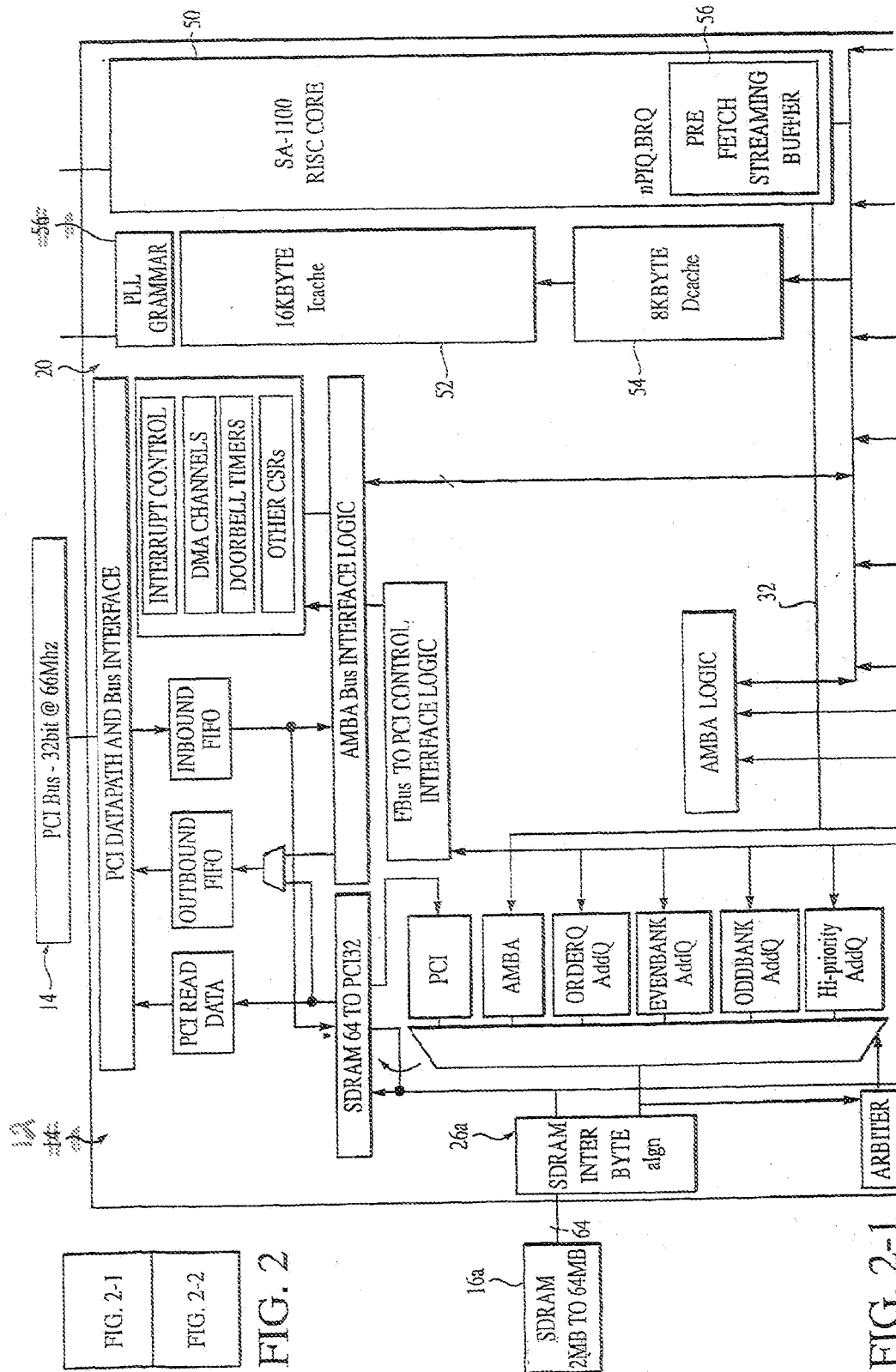
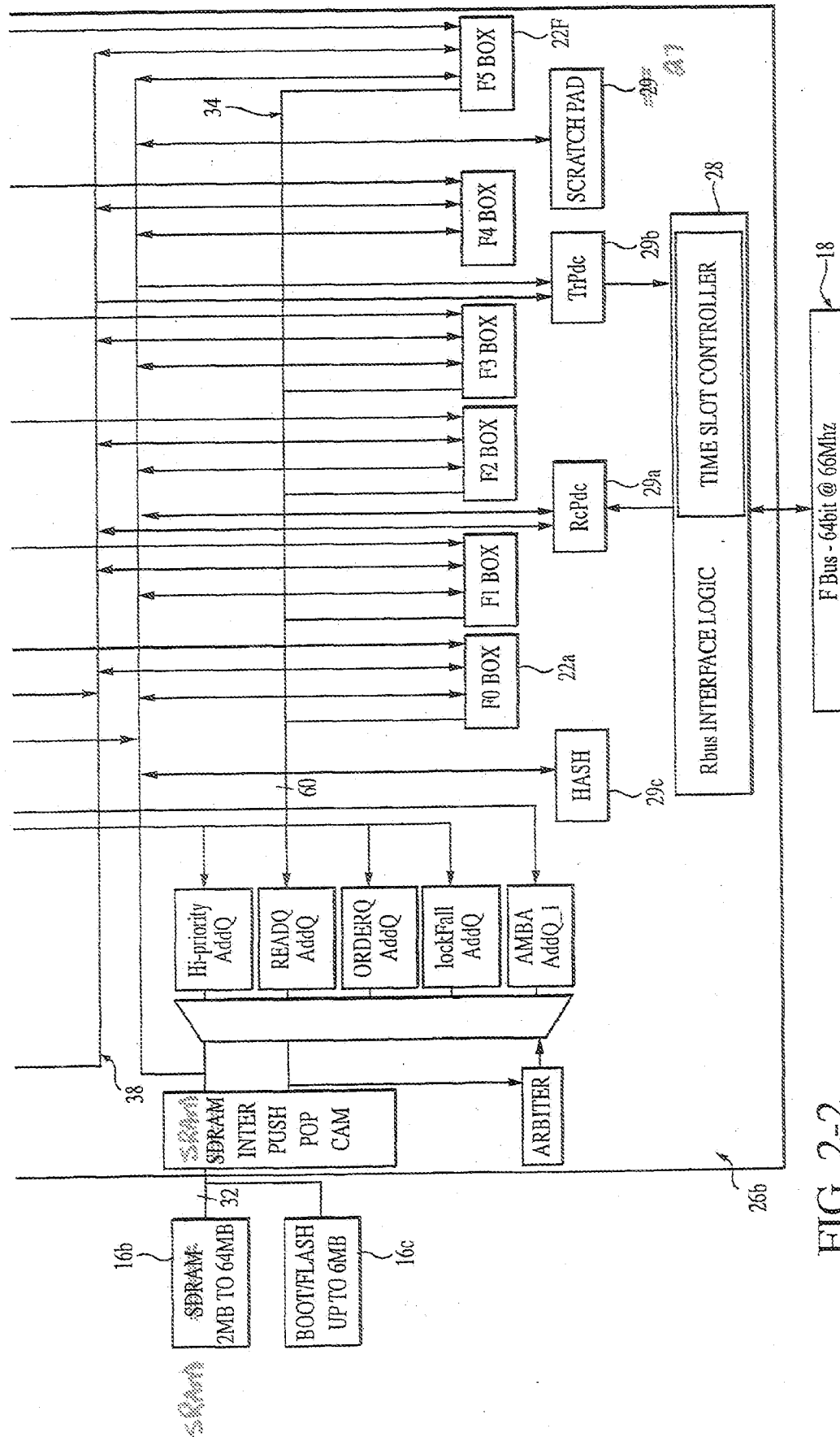


FIG. 2-1

Applicant(s): Gilbert Wolrich et al.  
DOUBLE SHIFT INSTRUCTION FOR MICRO ENGINE USED IN  
MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE



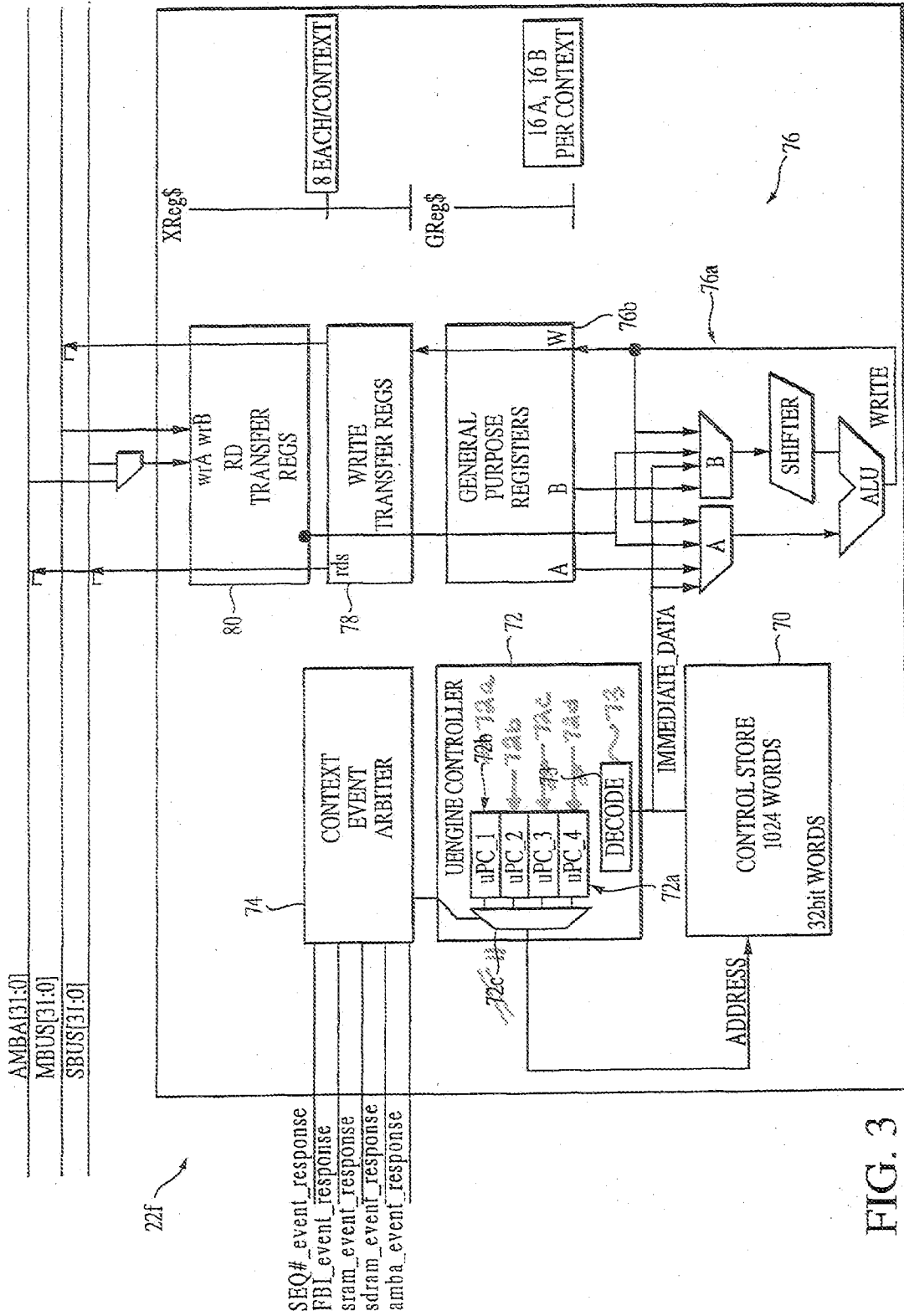
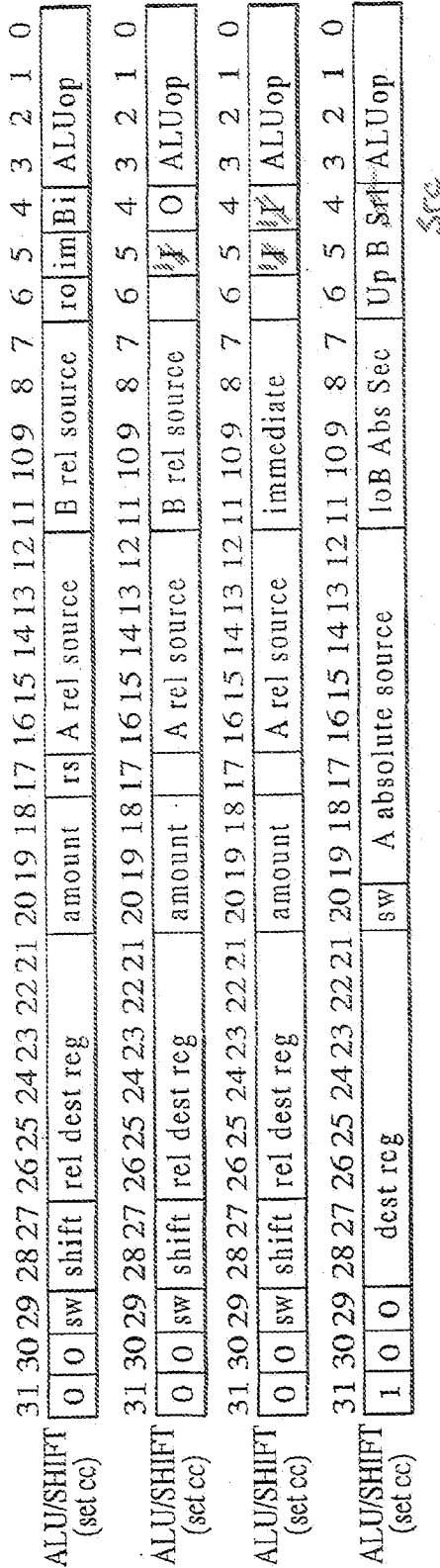


FIG. 3



Shift Decode:

(rs,r0) decode ([31:0] shifts into [63:32] and take [63:32]):

00 = left rotate

01 = right shift (32-ShfAmt = Right Shift Amt)

10 = left shift

11 = double shift ( upper A-op shifts into lower B-op)

====> "left rotate" of zero gives zero shift (therwise zero amount signifies indirect shift)

ALU-OP decode:

0000 = B

0001 = ~B

0010 = A&B (and)

0011 = A&~B (and~)

0100 = ~A&B (~and)

0101 = XOR

0110 = OR

0111 = mul-stuff

1000 = A-B

1001 = B-A

1010 =

1011 =

1100 = A+B(8)

1101 = A+B(16)

1110 = A+B

0011 = A+B+Cin

**FIG. 5**